AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-5. (Canceled).

6. (Currently Amended) A memory comprising:

a plurality of systolic memory arrays each divided into banks, each of the memory arrays arranged in a pipelined architecture and each of the plurality of systolic memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes; and

a plurality of pipeline registers, each register to couple to ~~one end~~ a first one of the banks of a corresponding one of the plurality of systolic memory arrays to provide read and write operations through a data pipe to the banks of the corresponding one of the systolic memory arrays beginning with the first one of the banks and to provide address access through an address pipe to the banks of the corresponding one of the systolic memory arrays beginning with the first one of the banks.

7. (Previously Presented) The memory of claim 6, wherein at least one of the plurality of data pipes is used for a reading operation.

8. (Previously Presented) The memory of claim 6, wherein at least one of the plurality of data pipes is used for a writing operation.

9. (Previously Presented) The memory of claim 6, each of the plurality of systolic memory arrays includes at least eight banks.

10. (Original) The memory of claim 6, wherein a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate.

11. (Previously Presented) The memory of claim 6, wherein a clock frequency and a data path width for the pipeline architecture is determined.

12. (Previously Presented) The memory of claim 6, wherein a number of pipeline stages relates to a number of clock cycles.

13. (Original) The memory of claim 12, wherein the number of pipeline stages is the same as the number of clock cycles.

14. (Previously Presented) The memory of claim 6, wherein each of the plurality of systolic memory arrays is divided into a horizontal arrangement.

15. (Previously Presented) The memory of claim 6, wherein each of the plurality of systolic memory arrays is divided into a vertical arrangement.

16. (Currently Amended) A memory comprising:

a plurality of systolic memory arrays each divided into banks, each of the systolic memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes, ~~wherein~~ and a writing operation into the memory is performed by pumping an address with data that is to be written into the memory; and

a plurality of pipeline registers, each register to couple to a first one of the banks of a corresponding one of the plurality of systolic memory arrays through a data pipe and an address pipe to provide read/write data input, data output and address access to the banks of the corresponding one of the systolic memory arrays through the first one of the banks arranged in the pipelined architecture.

17. (Currently Amended) The memory of claim 6, wherein a read operation from the memory is performed by pumping an address once and allowing the address to flow through ~~an~~ the address pipe to reach individual banks of one of the systolic memory arrays one cycle at a time.

18. (Previously Presented) The memory of claim 6, wherein memory operations from different banks having different memory addresses of one of the systolic memory arrays are interleaved.

19. (Previously Presented) The memory of claim 16, wherein peripheral access for one systolic memory array is accomplished from one side of the one systolic memory array.

20. (Original) The memory of claim 6, wherein whenever a bank receives a read address, memory access is initiated.

21. (Currently Amended) The memory of claim 6, wherein access latency for a bank is represented by 2i + L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents ~~the~~ cycles of latency to access the memory.

22. (Original) The memory of claim 21, wherein it will take i cycles to allow data to come out of the i th bank through a read pipeline.

23. (Currently Amended) The memory of claim 21, wherein to avoid memory collisions among data, a second read access of consecutive reads delays ~~the~~ placement of read result on the read data pipeline by a specified idle time.

24. (Original) The memory of claim 23, wherein the specified idle time is at least one clock cycle.

25. (Currently Amended) A processing system comprising:

a die including a microprocessor;

peripheral equipment coupled to the processing system;

a network interface; and

on-die or off-die systolic memory~~, the systolic memory~~ including:

a plurality of separate systolic memory arrays, each systolic memory array including a plurality of memory banks in a pipelined fashion, the plurality of memory banks of each systolic memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion, ~~wherein~~ and a read operation from the systolic memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks one cycle at a time, and

a plurality of pipeline registers, each register coupled to one of the separate systolic memory arrays, and each register is coupled to one end of a corresponding one of the systolic memory arrays to provide read data from the memory array, to provide write data to the array and to provide address information to the array.

26-27. (Canceled)

28. (Previously Presented) The processing system of claim 25, wherein each bank is associated with a mechanism to support addressing and data operations.

29. (Canceled)

30. (Currently Amended) The processing system of claim 25, wherein access latency for a bank is represented by 2i + L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents ~~the~~ cycles of latency to access the memory.

31-33. (Canceled)

34. (Previously Presented) The memory of claim 6, wherein each bank is associated with a mechanism to support addressing each data operations of the corresponding bank.

35. (Currently Amended) A memory comprising:

a plurality of separate systolic memory arrays, each systolic memory array including a plurality of memory banks in pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion, ~~wherein~~ and a read operation is performed by pumping an address and allowing the address to flow through the address line to reach individual banks of one of

the plurality of separate systolic memory arrays one cycle at a time, and access latency for one bank of one of the plurality of separate systolic memory arrays is represented by 2i + L, where i represents time it takes to allow an address to reach a desired i th bank and L represents cycles of latency to access the memory.

36. (Previously Presented) The memory of claim 35, further comprising:

a plurality of pipeline registers, each register to couple to one of the separate systolic memory arrays.

37. (Previously Presented) The memory of claim 35, wherein each bank is associated with a mechanism to support addressing and data operations.

38-39. (Canceled)

40. (Currently Amended) A memory comprising:

a plurality of separate systolic memory arrays, each systolic memory array including a plurality of memory banks in pipelined fashion, the plurality of memory banks of each systolic memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion, ~~wherein~~ and peripheral access for writing operations and addressing for one systolic memory array is accomplished from one side of the one systolic memory array and data for reading operations for the one systolic memory array is received from the one side of the one systolic memory array.